Deposited silicon high-speed integrated electro-optic modulator

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Abstract: We demonstrate a micrometer-scale electro-optic modulator operating at 2.5 Gbps and 10 dB extinction ratio that is fabricated entirely from deposited silicon. The polycrystalline silicon material exhibits properties that simultaneously enable high quality factor optical resonators and sub-nanosecond electrical carrier injection. We use an embedded $p^+n^-n^+$ diode to achieve optical modulation using the free carrier plasma dispersion effect. Active optical devices in a deposited microelectronic material can break the dependence on the traditional single layer silicon-on-insulator platform and help lead to monolithic large-scale integration of photonic networks on a microprocessor chip.

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References and links

1. D. A. B. Miller, "Rationale and challenges for optical interconnects to electronic chips," Proc. IEEE **88**, 728-749 (2000).
2. A. Shacham, K. Bergman, and L. P. Carloni, "Photonic Networks-on-Chip for Future Generations of Chip Multiprocessors," IEEE Trans. Comput. **57**, 1246-1260 (2008).
3. A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. Paniccia, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," Nature **427**, 615-618 (2004).
4. A. Liu, L. Liao, D. Rubin, H. Nguyen, B. Ciftcioglu, Y. Chetrit, N. Izhaky, and M. Paniccia, "High-speed optical modulation based on carrier depletion in a silicon waveguide," Opt. Express **15**, 660-668 (2007).
5. W. M. Green, M. J. Rooks, L. Sekaric, and Y. A. Vlasov, "Ultra-compact, low RF power, 10 Gb/s silicon Mach-Zehnder modulator," Opt. Express **15**, 17106-17113 (2007).
6. D. Marris-Morini, L. Vivien, J. M. Fédéli, E. Cassan, P. Lyan, and S. Laval, "Low loss and high speed silicon optical modulator based on a lateral carrier depletion structure," Opt. Express **16**, 334-339 (2008).
7. S. J. Spector, M. W. Geis, G. R. Zhou, M. E. Grein, F. Gan, M. A. Popovic, J. U. Yoon, D. M. Lennon, E. P. Ippen, F. Z. Kärtner, and T. M. Lyszczarz, "CMOS-compatible dual-output silicon modulator for analog signal processing," Opt. Express **16**, 11027-11031 (2008).
8. Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," Nature **435**, 325-327 (2005).
9. S. Manipatruni, X. Qianfan, B. Schmidt, J. Shakya, and M. Lipson, "High Speed Carrier Injection 18 Gb/s Silicon Micro-ring Electro-optic Modulator," in *Proceedings of Lasers and Electro-Optics Society* (IEEE, 2007), pp.537-538.
10. M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Ultralow power silicon microdisk modulators and switches," in *5th IEEE International Conference on Group IV Photonics* (IEEE, 2008), pp. 4-6.
11. J.-B. You, M. Park, J.-W. Park, and G. Kim, "12.5 Gbps optical modulation of silicon racetrack resonator based on carrier-depletion in asymmetric p-n diode," Opt. Express **16**, 18340-18344 (2008).
12. G. K. Celler and S. Cristoloveanu, "Frontiers of silicon-on-insulator," J. Appl. Phys. **93**, 4955-4978 (2003).
13. J. S. Orcutt, A. Khilo, M. A. Popovic, C. W. Holzwarth, B. Moss, H. Li, M. S. Dahlem, T. D. Bonifield, F. X. Kaertner, E. P. Ippen, J. L. Hoyt, R. J. Ram, and V. Stojanovic, "Demonstration of an Electronic Photonic Integrated Circuit in a Commercial Scaled Bulk CMOS Process," in *Conference on Lasers and Electro-Optics* (Optical Society of America, 2008), paper CTuBB3.
14. C. W. Holzwarth, J. S. Orcutt, H. Li, M. A. Popovic, V. Stojanovic, J. L. Hoyt, R. J. Ram, and H. I. Smith, "Localized Substrate Removal Technique Enabling Strong-Confinement Microphotonics in Bulk Si

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CMOS Processes," in *Conference on Lasers and Electro-Optics* (Optical Society of America, 2008), paper CThKK5.
15. K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," Proc. IEEE **89**, 602-633 (2001).
16. A. W. Topol, J. D. C. La Tulipe, L. Shi, D. J. Frank, K. Bernstein, S. E. Steen, A. Kumar, G. U. Singco, A. M. Young, K. W. Guarini, and M. Ieong, "Three-dimensional integrated circuits," IBM J. Res. and Dev. **50**, 491-506 (2006).
17. M. Beals, J. Michel, J. F. Liu, D. H. Ahn, D. Sparacin, R. Sun, C. Y. Hong, L. C. Kimerling, A. Pomerene, D. Carothers, J. Beattie, A. Kopa, A. Apsel, M. S. Rasras, D. M. Gill, S. S. Patel, K. Y. Tu, Y. K. Chen, and A. E. White, "Process flow innovations for photonic device integration in CMOS," Proc. SPIE **6898**, 689804 (2008).
18. R. Amatya, C. W. Holzwarth, H. I. Smith, and R. J. Ram, "Precision Tunable Silicon Compatible Microring Filters," IEEE Photon. Technol. Lett. **20**, 1739-1741 (2008).
19. M. W. Geis, S. J. Spector, R. C. Williamson, and T. M. Lyszczarz, "Submicrosecond submilliwatt silicon-on-insulator thermooptic switch," IEEE Photon. Technol. Lett. **16**, 2514-2516 (2004).
20. J. Liu, M. Beals, A. Pomerene, S. Bernardis, R. Sun, J. Cheng, L. C. Kimerling, and J. Michel, "Waveguide-integrated, ultralow-energy GeSi electro-absorption modulators," Nature Photon. **2**, 433-437 (2008).
21. T. Kamins, *Polycrystalline Silicon for Integrated Circuits and Displays,* 2nd ed. (Kluwer, 1998).
22. L. Liao, D. R. Lim, A. M. Agarwal, X. Duan, K. K. Lee, and L. C. Kimerling, "Optical transmission losses in polycrystalline silicon strip waveguides," J. Electron. Mater. **29**, 1380-1386 (2000).
23. S. Selvaraja, M. Schaekers, W. Bogaerts, D. V. Thourhout, and R. Baets, "Polycrystalline silicon as waveguide material for advanced photonic applications," in *Proceedings of 11th IEEE/LEOS Benelux Annual Workshop* (IEEE/LEOS, 2007), pp.19-20.
24. Q. Fang, J. F. Song, S. H. Tao, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Low loss (~6.45dB/cm) sub-micron polycrystalline silicon waveguide integrated with efficient SiON waveguide coupler," Opt. Express **16**, 6425-6432 (2008).
25. K. Preston, B. Schmidt, and M. Lipson, "Polysilicon photonic resonators for large-scale 3D integration of optical networks," Opt. Express **15**, 17283-17290 (2007).
26. K. Preston, P. Dong, B. Schmidt, and M. Lipson, "High-speed all-optical modulation using polycrystalline silicon microring resonators," Appl. Phys. Lett. **92**, 151104 (2008).
27. M. Dutoit and F. Sollberger, "Lateral Polysilicon p-n Diodes," J. Electrochem. Soc. **125**, 1648-1651 (1978).
28. S. V. Karnik and M. K. Hatalis, "Lateral polysilicon p+-p-n+ and p+-n-n+ diodes," Solid-State Electron. **47**, 653-659 (2003).
29. R. Soref and B. Bennett, "Electrooptical effects in silicon," IEEE J. Quantum Electron. **23**, 123-129 (1987).
30. C. R. M. Grovenor, "Grain boundaries in semiconductors," J. Phys. C **18**, 4079-4119 (1985).
31. S. Manipatruni, Q. Xu, and M. Lipson, "PINIP based high-speed high-extinction ratio micron-size silicon electrooptic modulator," Opt. Express **15**, 13035-13042 (2007).
32. Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, "12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators," Opt. Express **15**, 430-436 (2007).
33. Q. Xu, D. Fattal, and R. G. Beausoleil, "Silicon microring resonators with 1.5-μm radius," Opt. Express **16**, 4309-4315 (2008).
34. J. S. Foresi, P. R. Villeneuve, J. Ferrera, E. R. Thoen, G. Steinmeyer, S. Fan, J. D. Joannopoulos, L. C. Kimerling, H. I. Smith, and E. P. Ippen, "Photonic-bandgap microcavities in optical waveguides," Nature **390**, 143-145 (1997).
35. B. Schmidt, Q. Xu, J. Shakya, S. Manipatruni, and M. Lipson, "Compact electro-optic modulator on silicon-on-insulator substrates using cavities with ultra-small modal volumes," Opt. Express **15**, 3140-3148 (2007).
36. A. T. Voutsas, "Laser Crystallization of Thin Films for Flat Panel Display Applications," in *Recent Advances in Laser Processing of Materials*, J. Perriere, E. Millon, and E. Fogarassy, eds. (Elsevier, New York, 2006), pp. 317-373.

1. Introduction

Photonic networks on a silicon microelectronic chip offer the opportunity to overcome the power and bandwidth limitations in traditional microprocessor interconnects [1, 2]. One critical device for on-chip optical networks is a silicon high-speed waveguide-integrated electro-optic modulator, which converts data from the electrical domain to the optical domain. All previous examples of these modulators (including interferometer [3-7] and microresonator [8-11] geometries) have been fabricated on single-crystalline silicon-on-insulator (SOI) [12]. Reliance on the SOI platform presents two difficult challenges for the integration of optics with microprocessor chips. First, the large-scale integration of hundreds of optical devices

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would take a prohibitive amount of real estate away from transistors in the same silicon layer, and second, the buried oxide thickness in standard microelectronic SOI is much smaller than the optical wavelength and therefore not appropriate for a waveguide cladding [13, 14]. Here we show the first demonstration of GHz-speed electro-optic modulation in a deposited microelectronic film. The use of deposited material, here polycrystalline silicon (polysilicon), would enable the monolithic integration of optics in a separate layer of a microprocessor chip and provide the flexibility needed for optical system design.

The requirements for both chip real estate and device compatibility indicate that photonic devices and electronic devices should be on separate layers of a microprocessor chip [15]. One option for multilayer integration is to fabricate separate electronic and photonic SOI wafers followed by wafer thinning, bonding, and metallization to connect the layers, however the required processes are not yet cost effective and are therefore not in current production [16]. A simpler, monolithic approach would be to deposit silicon-based layers above the transistor layer and process them into optical devices [17]. Previous active switching or modulating devices in deposited microelectronic films such as silicon nitride or amorphous silicon have relied on the thermo-optic effect [18] which is limited to low speeds in the MHz regime [19]. Liu et al. recently demonstrated a GHz-speed, epitaxially grown GeSi electro-absorption modulator integrated with CMOS circuits [20], however epitaxial growth typically requires a crystalline seed which limits where the material can be grown.

In this work we show integrated electro-optic devices in deposited polysilicon, a standard microelectronic material containing crystalline grains separated by thin amorphous grain boundaries [21]. Previous optical devices in the polysilicon-on-insulator material system included passive waveguides with loss on the order of 10 dB/cm [22-24], optical filters [13, 25], and a recent demonstration of all-optical modulation [26]. Here we demonstrate electro-optic functionality by embedding a p^+-n^--n^+ diode [27, 28] around a polysilicon ring resonator as shown in Fig. 1. In order to achieve good optical and electrical properties, we use photonic structures with cross sectional dimensions of hundreds of nanometers, on the order of the material grain size [26]. This enables sub-nanosecond carrier injection and optical modulation using the free carrier dispersion effect [29].

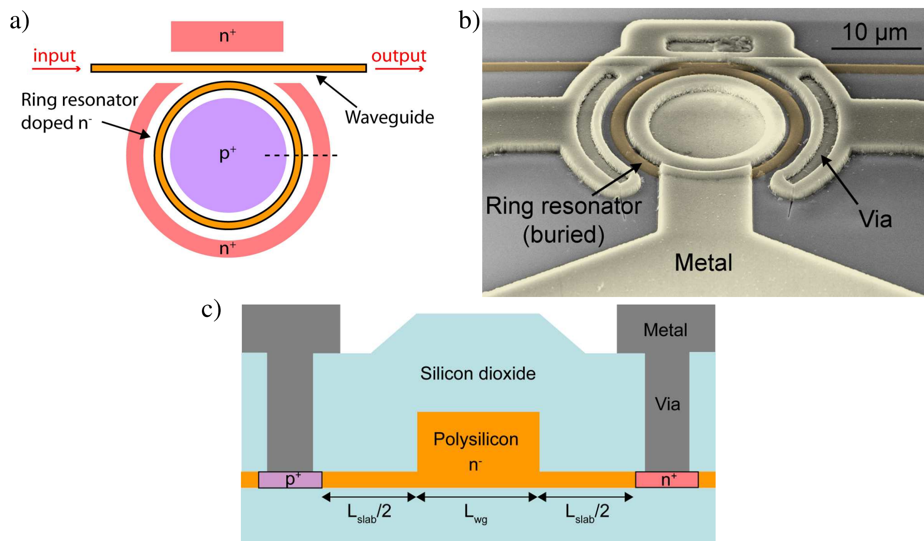

Fig. 1. Polysilicon electro-optic modulator device structure. (a) Top view schematic showing the doping regions of the device that form a p^+-n^--n^+ diode around a ring resonator. (b) Tilted view colorized scanning electron microscope (SEM) image. The polysilicon resonator and 450 nm-wide bus waveguide are buried under 1 μm silicon dioxide. (c) Cross-section schematic of the device (not to scale).

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2. Polysilicon material properties and device fabrication

The polysilicon material system differs from single-crystalline silicon in three critical ways that affect electro-optic modulator design and performance: effective carrier mobility (μ_{eff}), effective free carrier lifetime (τ_{fc}), and optical loss. All three parameters are affected by the grain boundaries that exist throughout the material. For instance, grain boundaries in polysilicon present a potential barrier to the flow of carriers which results in decreased effective carrier mobility μ_{eff} [21, 30]. Mobility in various phases of silicon ranges from the order of 1,000 $cm^2/V{\cdot}s$ (single crystalline silicon) to less than 1 $cm^2/V{\cdot}s$ (amorphous silicon).

Background doping of the device region is required to ensure sufficient charge injection because intrinsic undoped polysilicon is extremely resistive (corresponding to low mobility μ) [21]. An increase in doping above the grain boundary trap density improves the electrical injection [21, 28], but this is a tradeoff with increased optical loss due to free carrier absorption [29]. In doped polysilicon, some percent of dopant atoms segregate to low energy positions at the grain boundaries where they do not contribute carriers. Additionally, the carriers themselves can fill in grain boundary trap states [21] where they will not contribute to free carrier dispersion. To keep the background free carrier losses low, we conservatively choose an average n-type doping level $N_d \approx 2{\cdot}10^{17}$ cm^{-3}. We estimate that this produces a free carrier concentration $n \leq 10^{17}$ cm^{-3} which keeps excess free carrier loss below 4 dB/cm [29].

Grain boundaries and other intragrain defects in polysilicon induce a fast carrier recombination lifetime, which allows a polysilicon modulator to reach a steady state carrier concentration faster than a comparable crystalline silicon device. This lifetime was measured in previous work to be on the order of $\tau_{fc} \approx 100$ ps for a grain size of approximately 300 nm in a 450 nm by 250 nm channel waveguide [26]. In addition to decreased τ_{fc} and μ_{eff}, optical losses are moderately increased in polysilicon due to scattering and absorption of light at the grain boundaries [22], though resonator quality factors of 20,000 are achievable [25] which is more than sufficient for a modulator device [9].

Fabrication of the devices is performed using standard microelectronic processes. We start with a silicon wafer and grow a 3 µm thermal oxide isolation layer. We then deposit a 270 nm layer of amorphous silicon by low pressure chemical vapor deposition (LPCVD) at 550°C and crystallize the film into polysilicon by a thermal anneal at a maximum temperature of 1100°C. Background doping of the resonator area is done by opening windows in positive e-beam resist and performing Phosphorus ion implantation with a dose of $4.7{\times}10^{12}$ cm^{-2} and energy of 130 keV. We pattern waveguides and resonators using e-beam lithography and XR-1541 resist, and transfer the pattern using chlorine-based inductively coupled plasma reactive ion etching (ICP-RIE), leaving a 40 nm slab of silicon for electrical access. We dope p^+ and n^+ contact regions in the slab by BF_2 and Phosphorus ion implantation at $1.2{\times}10^{15}$ cm^{-2} dose and clad the structures in 1 µm silicon dioxide by plasma enhanced chemical vapor deposition (PECVD). We then anneal the sample in N_2 for 30 minutes at 600°C, 15 minutes at 900°C, and 15 seconds at 1050°C for silicon regrowth and dopant activation. (By ending with the high temperature rapid thermal anneal, we maximize the number of dopant ions that are electrically active [21].) Finally we open vias to the contact regions in order to form nickel silicide contacts and aluminum pads using e-beam evaporation and liftoff steps. The device consists of a 10 µm radius polysilicon ring resonator embedded in a 40 nm tall p^+-n^--n^+ diode and laterally coupled to a polysilicon waveguide. A cross-sectional schematic, top view schematic, and top view microscope image are shown in Figure 1.

3. Results

We first analyze the electro-optic device with DC measurements. Optical measurements are performed using a tunable infrared laser coupled through a polarization controller to a tapered lens fiber. Light is coupled on and off chip via nanotaper mode converters. Output from the chip is collected by an objective lens, passed through a polarization filter, and focused on a photodetector. Figure 2(a) shows a measured resonance at $\lambda_0 = 1550.35$ nm with spectral 3 dB width $\Delta\lambda_{FWHM} = 0.45$ nm, quality factor $Q = \lambda_0/\Delta\lambda_{FWHM} = 3{,}400$ and 16 dB extinction ratio.

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Other devices from this fabrication run exhibited quality factors exceeding 10,000. We perform a DC electrical measurement on the device to obtain a diode IV curve shown in Fig. 2(b). The device exhibits an on-resistance of approximately 3.5 kΩ, which includes contact resistance at the p^+ and n^+ regions and series resistance through the lightly doped waveguide and slab regions.

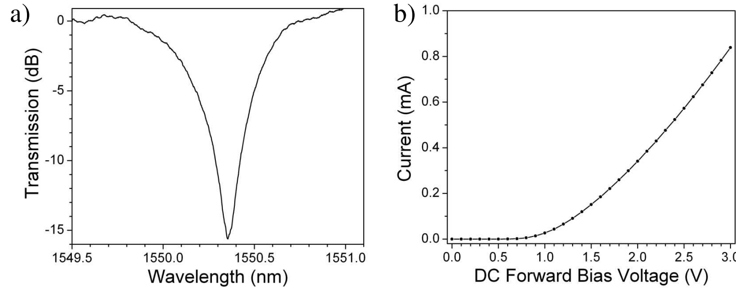

Fig. 2. DC optical and electrical measurements. (a) Wavelength scan showing through port transmission for quasi-TM polarization with quality factor $Q = \lambda_0/\Delta\lambda_{FWHM}$ = 3,400 and 16 dB extinction ratio. (b) Electrical IV curve demonstrating DC diode characteristics.

We demonstrate 2.5 Gbps modulation and measure a 10 dB modulation depth with a NRZ 2^7-1 PRBS electrical signal applied with a ±4V swing and a 4V DC bias. For AC measurements, output light from the chip is collimated, coupled to a fiber, passed through a fiber pre-amplifier and tunable filter, and recorded by an oscilloscope with a 20 GHz photodetector. The oscilloscope is triggered to the pattern generator which provides the NRZ electrical signal to a high-speed amplifier and bias T circuit. By forward biasing the diode and injecting free carriers into the ring, the resonant wavelength blue shifts and changes the probe wavelength transmission from low to high. Figure 3(a) and (b) show the optical transmission and frame-averaged optical eye diagram when the wavelength is tuned to minimize the off-state transmission. The slight overshoot and oscillation of the high transmission of the waveform in Fig. 3 is caused by electrical impedance mismatch, coupled with the fact that the voltage swing here is not sufficient to reach full optical transmission. Comparing the measured 10 dB extinction ratio in Fig. 3(a) to the 16 dB extinction on resonance in Fig. 2(a), we estimate a 6 dB insertion loss and a maximum wavelength shift $\Delta\lambda \approx 130$ pm. This $\Delta\lambda$ corresponds to an effective index shift $\Delta n_{eff} = n_g\, \Delta\lambda/\lambda_0 = 3.66\times10^{-4}$ given a group index n_g = 4.36 found with a finite difference modesolver program. Based on modesolver simulation, this Δn_{eff} is caused by a silicon refractive index change $\Delta n = 3.7\times10^{-4}$, which is caused by a carrier injection level $\Delta N = \Delta P = 8.4\times10^{16}$ cm^{-3} [29]. We estimate energy consumption of 950 fJ/bit and power consumption of 2.4 mW based on the voltage swing, bit rate, carrier lifetime, device size, and charge injection levels.

The carrier mobility μ can be estimated from the measured DC on-resistance using the formula [28]:

$$R_{on} = \frac{1}{q\mu n w}\left(\frac{L_{slab}}{h_{slab}} + \frac{L_{wg}}{h_{wg}}\right) \tag{1}$$

where q is the electron charge, n is the free carrier concentration (~10^{17} cm^{-3}), w is the circumference of the ring (62.8 μm), L_{slab} is the total cross-section length of the slab region between the n^+ and p^+ regions (1.55 μm), L_{wg} is the width of the waveguide (0.45 μm), h_{slab} is the height of the polysilicon slab (40 nm), and h_{wg} is the waveguide height (270 nm). By attributing the full 3.5 kΩ to material resistance, we calculate a first-order lower bound for the carrier mobility μ = 100 cm^2/V·s. This is only one order of magnitude lower than values in crystalline silicon [21], which explains why the electrical performance can approach that seen in crystalline SOI devices.

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We model the operation of the device using Silvaco Atlas simulation software and show excellent agreement with experimental results. As a first order model of the effect of grain boundaries on the polysilicon electrical properties, we define silicon bulk material properties within our device, including a free carrier lifetime τ_{fc} = 80 ps and an effective carrier mobility μ_n = 100 cm^2/V·s for electrons and μ_p = 50 cm^2/V·s for holes. We use Shockley-Read-Hall and Klaassen models for carrier recombination and mobility, and the surface recombination velocity is taken to be 16,000 cm/s which is consistent with SOI modeling [31]. We apply the same voltage signal as was used in Fig. 3(a) (without ringing) and solve for the transient charge concentrations ΔN(t) and ΔP(t) in the waveguide region. These values are then converted to a wavelength shift $\Delta\lambda$(t) and excess loss $\Delta\alpha$(t) which are put into a Lorentzian resonance model to find the optical response. Note that a time domain optical model is not required because the cavity photon lifetime $\tau_p = Q\lambda/(2\pi c)$ = 2.7 ps is much less than the charge injection time. The result for optical transmission is shown in Fig. 3(c), which demonstrates excellent agreement in rise time, fall time, and extinction ratio with the experimental results in Fig. 3(a).

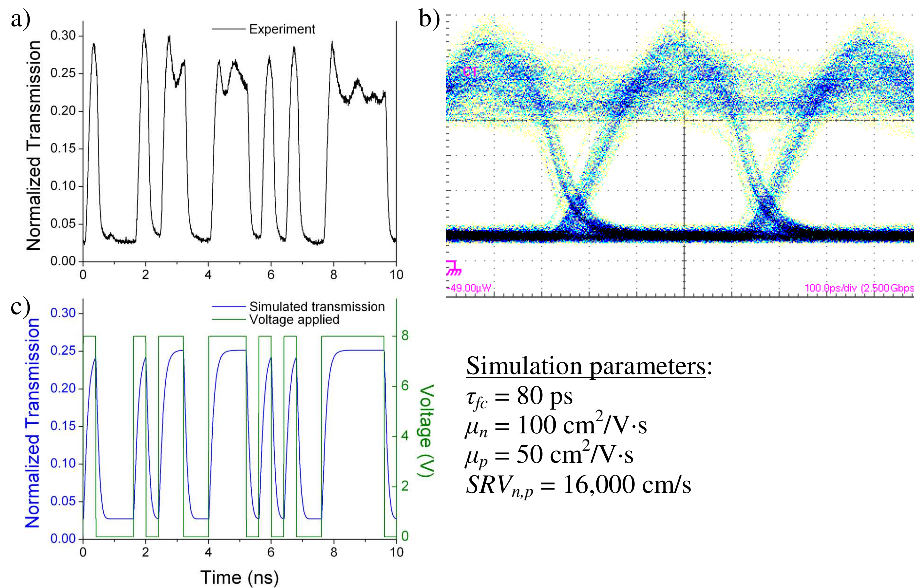

Fig. 3. Electro-optic response of the polysilicon modulator. (a) Optical transmission and (b) frame-averaged optical eye diagram for NRZ 2.5 Gbps 2^7-1 PRBS signal. (c) Simulation of electro-optic response using bulk distributed material parameters τ_{fc} = 80 ps, μ_n = 100 cm^2/Vs, and μ_p = 50 cm^2/Vs.

4. Discussion

The polysilicon device shown here demonstrates speed and energy consumption (2.5 Gbps and 950 fJ/bit) approaching those in state-of-the-art crystalline silicon microresonator devices (~ 20 Gbps and ~ 100 fJ/bit [9, 10]). The reduced carrier mobility μ in polysilicon necessitates the use of a slightly higher forward bias voltage for the on-state which increases power consumption, however this is partially compensated by the fast carrier recombination [26] which eliminates the need for a reverse bias voltage for the off-state. The optical transmission in Fig. 3 exhibits a 90%-10% fall time of 120 ps with 0V applied for the off-state. The 10%-to-90% rise time in Fig. 3 is 150 ps, indicating a possible bit rate > 5 Gbps. With moderately improved Q and electrical characteristics, we expect the insertion loss could be reduced to near 0 dB and the speed increased to tens of Gbps using pre-emphasis techniques [32].

Electrical properties of the device can be improved by two main approaches: optimizing the background doping concentration and decreasing the device size. The background doping strongly influences the electrical mobility and resistance obtained in the film, which in turn

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strongly affect the speed and power consumption [21, 30]. Optimal conditions may be found at a higher doping concentration N_d that further improves the mobility without negatively affecting off-state Q. Energy consumption can be greatly reduced to potentially tens of fJ/bit by decreasing the size of the resonator to smaller microring [33] or 1-D cavity geometries [34, 35], since switching energy scales inversely with resonator size [33].

The primary consideration for photonic integration with the CMOS process flow is the temperature required for device fabrication [17]. The highest temperature in our process is the 1100°C crystallization anneal which is used to maximize the grain size and minimize the optical loss [22]. Because of the relatively high temperature, these devices would need to be fabricated before any doping or silicidation is performed on the silicon transistor layer. Note however that a high temperature thermal anneal is not fundamentally required for large grain polycrystalline films. Crystallization by nanosecond excimer laser annealing can be used to achieve grain sizes of micrometers without any steady state heating of the substrate. This technique is currently used extensively in the thin film transistor industry to produce polycrystalline films on glass and plastic substrates [36]. With a low-temperature process below 450°C, active polysilicon devices could be integrated with low loss amorphous silicon or silicon nitride waveguides on top of the CMOS metal interconnect layers. This type of post-backend processing would enable optical functionality on a CMOS chip with minimal changes to the microelectronic process flow.

5. Conclusion

For the first time to our knowledge, we have demonstrated GHz-speed electro-optic modulation in a deposited microelectronic material. The polycrystalline silicon exhibits optical and electrical properties which enable modulation of the transmission through a microring resonator on a 150 ps timescale. This work represents a step towards adapting high-performance silicon photonic devices for monolithic large-scale integration with standard CMOS microelectronics.

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